REMARKS

Pending Claims

Claims 1-17 are pending in this application. Claims 1, 7, 9 and 15 have been amended. No new matter has been added.

Drawing Objections

The drawings have been objected to under 37 C.F.R. §1.83(a), which requires that the drawings show every feature of the invention specified in the claims. Applicants respectfully assert that the drawings show each feature of the claimed invention as follows.

With respect to claim 6, the switch MOS is shown in Fig. 7, which shows an MOS disposed between a memory cell (MA) and a sense amplifier (AMP). In particular, SLSW designates a layout of the switch M2 and re1 designates a signal for controlling M2. See page 16, lines 1-20 of the specification.

As to claims 7 and 8, the access circuit and switch (MOS) that are specified in claim 7 are shown in Fig. 11. See, the Brief Description of the Drawings for Fig. 11 on page 6, lines 19-20, which explains that a peripheral circuit for accessing the memory cells to which the present invention is applied is shown in the figure. With respect to claim 8, the access circuit for accessing to the memory cells of the memory cell array (MA) is composed of cells (DEC, WDR, CONT, WA, YS, SA) and switch MOS's, e.g. MS4 and MS6. The first switch MOS is shown by MS4 and the second switch by MS6.

Regarding support in the drawings for the threshold voltages of claim 13, Fig. 10 shows a table of threshold voltages labeled as "CASE2", "CASE3" and "CASE4"

in the figure. In particular, the absolute value of the threshold voltages of the transfer MOSFET (MT 1, MT 2) and the driver MOSFET (MD 1, MD 2) is lower than an absolute value of a threshold voltage of the load MOSFET (ML1, ML2), as shown in the table. Additionally, Fig. 10 shows the threshold voltages specified in claim 14 as "CASE4".

The features of the second paragraph of claim 15 are shown in Fig. 9, which shows a layout diagram of the end of a memory cell array. Each area MC of Fig. 9 encircled by narrow broken lines denote one memory cell, which is comprised of 6 MOS transistors that are, in turn, encircled by respective bold broken lines. Additionally a transistor having a gate indicated by Vss and a transistor having a gate indicated by refl are located in the area that is not surrounded by the broken lines (a first area) in Fig. 9, respectively. As to claim 16, the area surrounded by the dotted line in Fig. 9 shows a memory cell, as aforementioned, and the gate patterns located in the area are symmetrically disposed with respect to a certain point, which is readily discerned by inspection of the figure. With regard to claim 17, the transistor having the gate indicated by ref 1 that is located in the area that is not surrounded by the dotted line (a first area) in Fig. 9 corresponds to the switch specified in the claim.

Applicants respectfully assert that each of the elements of the invention as claimed is shown in the drawings, for the reasons stated in the foregoing discussion. Accordingly, Applicants request that the objection to the drawings be withdrawn.

Claim Objections

Claims 1, 9 and 15 have been amended in order to overcome the claim objection which states that the connective relationship of the driver MOSFET, the

transfer MOSFET, and the load devices is not defined. In response, Applicants have amended each of the independent claims to state that the static type memory cells are comprised of a latch circuit including a pair of driver MOSFETs and a load device and two transfer MOSFETs accessing to the latch circuit. Accordingly, the connective relationships are established in the claim language and therefore the objection to the claims should be withdrawn.

Claim 7 has been amended to delete the memory cell array since it had already been defined in claim 1, as kindly noted by the Examiner.

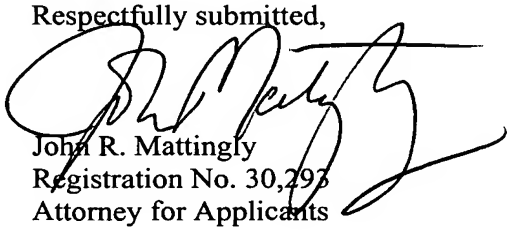
Allowable Subject Matter

Applicants thank the Examiner for the indication of the allowability of claims 1-17.

Conclusion

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



John R. Mattingly
Registration No. 30,293
Attorney for Applicants

JRM/so
MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.
1800 Diagonal Rd., Suite 370
Alexandria, Virginia 22314
(703) 684-1120
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